Characterization and Model of High Quality Factor and Broadband Integrated Inductor on Si-Substrate

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Abstract **— Proton bombardment has been used to boost the on-chip inductor quality factor and to also improve the frequency response. In this paper we demonstrated these advantages using the 0.13μm and 0.18μm RF CMOS processes. Based on the model, we evaluated how the performance improved using bombardment technology. A simultaneously impressive increase both in the peak Q-value and the optimal frequency have been evidenced due to its significantly reduced substrate parasitic effect as a result of higher substrate resistivity. This can be considered as a solution to integrate inductor on a Si substrate.**

I. INTRODUCTION

With the explosive growth of the wireless communication market, CMOS has emerged as the strongest candidate to meet the demands of a low-cost, high integration and mature technology. However, manufacturing on-chip inductors with a high quality factor (Q) in a standard silicon technology presents a difficult task, due to its substrate loss and limited metal thickness. Therefore, many approaches have been proposed to boost the Q of the inductor on a low-resistivity Si substrate. These include using higher conductivity metal layers to reduce the loss resistance of the inductor [1] and stacking several metal layers together in a multilevel metal process to increase the effective thickness of the spiral inductor [2]. These solutions are basically focused on reducing the metal conduction loss, therefore improving the associated Q-value in the low frequency regime. There are many other approaches that have been proposed as a way to reduce loss in the substrate at high frequency. These include inductors with a pattern ground shielding [3], with multi-level interconnect processes [4] to isolate the inductor from the lossy substrate, resulting in an elimination of the wave propagation loss in the substrate, thereby improving the associated Q-value. No doubt these techniques will definitely result in an improvement in the Q of inductors, however, due to the higher substrate losses of silicon compared to GaAs material, it makes the realization of a high Q inductor difficult. Ashby et al. have proposed a solution to effectively realize high-Q inductor on high-resistivity Si substrate effectively [5]. The simple solution of changing to a bulk P-substrate enables the fabrication of high-Q inductor, but may necessitate a price in reduced device density and possible yield loss. The resulting shift in device characteristics and new design rules to satisfy the new latch-up conditions would require a redesign of libraries, thereby voiding many of the re-use advantages in superchip integration. Based on the work of Lee et al. [6], we have combined the thick top Cu(Al) metal and high-level metal system with selective high energetic proton bombardment in order to obtain an improved Q and better frequency response thereby creating a high Q and broadband on-chip inductor. In this paper, we characterized and modeled the inductor to evaluate how the performance improved using this bombardment technology.

This paper is organized as follows: Section II describes the design of experiment, section III depicts the characteristics of the bombardment inductor, and section IV presents the inductor model and experimental results. Finally, we add some concluding remarks.

II. DESIGN OF EXPERIMENT

The current work follows the previous work of [6], but provides improvement on some crucial points. To better understand the interest of this bombardment we present an in-depth investigation of monolithic inductors in order to obtain improved performance. Please refer to [6] for details regarding the bombardment process.

Two types of layer configuration are investigated in this new work: the first involve an 8-level configuration with a 3 μm-thick top Cu-interconnect process. The second uses a 6-level configuration with a 2 μm-thick top Al-interconnect process. Both are commercially available using TSMC 0.13μm and 0.18μm RF CMOS processes in

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order to achieve both a small inductor resistance and minimal substrate loss due to the increased spacing of the silicon. Low-resistivity Si substrate with resistivity ranging from 8-12 Ω, was used in this study. The realized square inductor features a constant inner diameter, di=60um, a constant width, w=15um, and a constant spacing, s=2(1.5)um, with turns of N=1.5, 2.5, and 3.5.

Proton bombardment is performed with an aluminum mask in order to shield against MeV proton prior to its packaging and is used to pattern semi-insulating regions on a silicon wafer for RF ICs. To meet the penetration requirements of the entire Si, proton energy of several tens MeV is imposed to give a bombarded depth more than 40 mil. Following the proton bombardment, Van der Pauw method was employed to study the implantation effect on the substrate resistivity. Hot plate heat treatment at 150°C was imposed on the IC wafers to study the isothermal annealing effect on the devices. The S-parameters of the inductors were characterized and modeled in order to evaluate how the performance improved using the bombardment technology.

III. MEASUREMENT RESULTS

The measured resistivity in the range of 10^5 ~ 10^6 Ω-cm after the proton bombardment, on wafers of initial resistivity of about 10 Ω-cm, was achieved and is close to GaAs and intrinsic Si. This high resistivity is due to high defect densities, created by the bombardment, that effectively trap free carriers and increase resistivity. To study the stability of this high resistivity, we conducted a resistivity lifetime measurement. After the 150°C 1000 hour annealing, there is no significant resistivity degradation in order of magnitude, which suggests that high resistivity can be maintained. This high resistivity stable after 150°C annealing for 1000 hours, can be considered to simulate the reliability testing process.

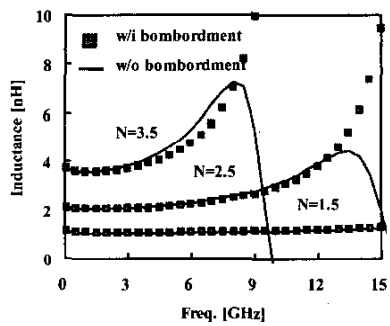

Fig. 1. Comparison of the effective inductance obtained from the 0.13μm inductors with and without proton bombardment.

S-parameters of inductors were measured with an Agilent-8510C Vector Network Analyzer (VNA). Based on the real and imaginary parts of the Y-parameters, the effective resistance (real part) and inductance (imaginary part) versus the frequencies can be extracted. The associated Q-value can be determined by the ratio of the imaginary part to the real part of the one-port input impedance transformed from the measured de-embedded S-parameters. Fig. 1 shows firstly the effective inductance of spiral inductors with and without bombardment in terms of 0.13μm technology. Experimental results show that is no impact on the inductance value over a large frequency range whether the bombardment is present or not. This result demonstrates that the bombardment does not disturb the magnetic field. Spiral inductors with various turns were also investigated. The value of the effective inductance ranged from 1.1nH up to 2.0nH and 3.5nH, which corresponds to N=1.5, 2.5 and 3.5 turns, respectively. As to the evaluation in Q value, Figs. 2(a) and (b) show the comparison between the two different layer configurations, namely 0.13μm and 0.18μm, when evaluating the Q value. As can be seen, at low frequencies, the Q values increase versus frequencies at the same slope for all inductors with or without bombardment. This is determined by the ohmic conducting mechanism and translates to the fact that the coil metal resistance was not changed after the bombardment. Inductors with more turns have higher Q values at low frequencies due to their larger inductance. However, Q values move downward by further increasing the frequencies, which is associated with the substrate parasitic effect dominating at higher frequencies. It, therefore, forms a peak Q value in Figs. 2(a) and (b). An abnormal result was observed in the Q factor of the 1.5 turn inductor with bombardment at high frequency. The reason for this abnormal result is not clear at this time. A comparison in the figure-of-merits including the peak Q value, the optimum frequency and the 3-dB bandwidth (BW) at the optimum frequency is summarized in Table 1. The peak Q value increased and shifted slightly to the high-frequency end for standard inductors with less turns, which is associated with a reduced substrate parasitic effect causing this increase and shift. A simultaneously impressive increase in the peak Q-value and a shift in the optimal frequency have been demonstrated in terms of bombardment. This is due to its significantly reduced substrate parasitic effect resulting from higher substrate resistivity and this will be evidenced in terms of an inductor model described in the next section. A maximum Q value of more than 20 and 15 is achieved at an optimum frequency as high as 6.5 GHz and 8 GHz in the case of 0.13μm and 0.18μm, respectively. These are evident in an improvement in both the peak Q-value and

the broadbanded frequency response that can be achieved. Significant improvements both in the peak Q-value and BW, as high as 50% on average, have been effectively demonstrated. The higher peak Q-value with the 0.13μm inductor is due to the use of low resistivity Cu. The higher optimum frequency associated with the inductor of 0.18μm and is due to its higher dielectric thickness despite having fewer metal layers.

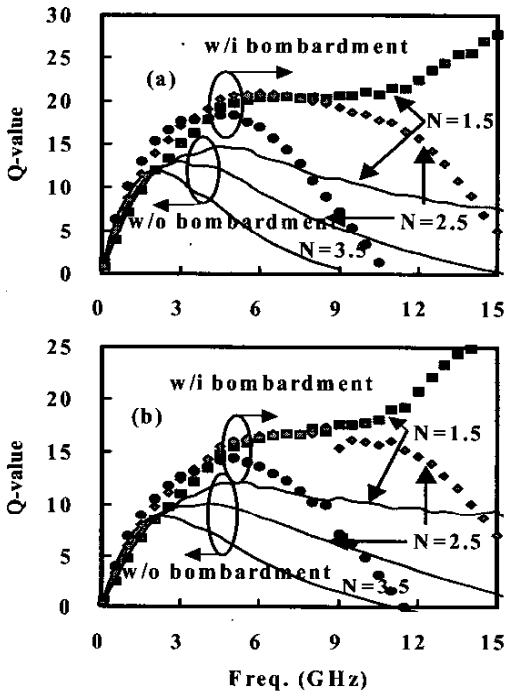

Fig. 2. Comparison of the Q value for inductors with and without proton bombardment, obtained from, (a) the 0.13μm, (b) the 0.18μm.

Table I. Comparison of the inductors characteristics with and without proton bombardment.

Inductor		Qpeak/GHz		ΔQ_{peak}	BW (GHz)		ΔBW
Process	N	Std.	Hi-Q	(%)	Std.	Hi-Q	(%)
0.13μm	1.5	14.6/4.3	20.7/6.8	42	3.9	N.A.	N.A.
	2.5	13.1/3.1	20.6/6.6	58	2.9	5.6	93
	3.5	11.8/2.1	18.5/4.1	57	2.1	3	43
0.18μm	1.5	11.8/5.2	17.1/8.3	45	6.3	N.A.	N.A.
	2.5	10.2/3.7	16.9/8.1	66	4	6.2	55
	3.5	8.8/2.4	14.1/4.9	60	2.7	3.9	44

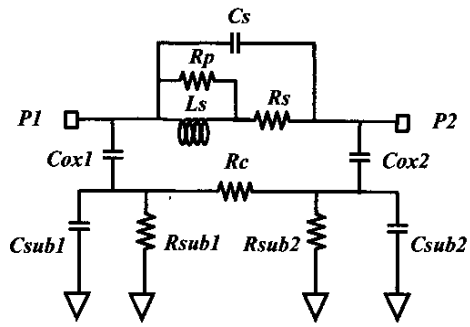

Fig. 3. Lump equivalent circuit model of spiral inductor on Si substrates.

IV. INDUCTOR MODEL

In addition to direct calculation from measured S-parameters, we also established an equivalent circuit model. A single π-type lumped-element equivalent circuit model, shown in Fig. 3, has been used to fit experimental measurements of silicon monolithic inductors. For these spiral inductors, the equivalent circuit model provides an analytic tool in order to identify the improved factors caused by the bombardment approach. The series branch consists of the series inductor Ls, the series resistor Rs, and the series feed forward capacitor Cs. Two parallel branches represent parasitics of port-1 and port-2. The capacitor Cox represents the capacitance between the spiral turns of the inductor and the substrate. Csub and Rsub model the silicon substrate and can be extracted from the measurement data. Furthermore, substrate shunting resistor, Rc, and the skin-effect resistor, Rp, were added to further improve the fit.

To determine the unknown circuit parameters, we simplified the two-port equivalent circuit as a simple π-model and then calculated the series and shunt branches from the Y-parameter. By taking the real and imaginary parts of Y12, equivalent inductance and resistance were extracted. Similarly, input and output shunt capacitance and resistance to substrate may be extracted by taking the real and imaginary parts of Y11+Y12 and Y22+Y12. By minimizing the difference between the model and the measurement, we applied a "best fit" procedure, based on the least square minima method, to each of the branches separately so as to obtain the estimated parameter values. The elements of the equivalent circuit model listed in Table II were then determined from the two-port S-parameters optimization procedure for the various inductors with and without bombardment. In Figs. 4(a) and (b), the simulation results for the extracted inductance

and Q-factor, by using the equivalent circuit shown in Fig. 3 with extracted values shown in Table II, are compared with the measured data for various inductors with proton bombardment in the case of 0.13μm. Excellent agreement was found for all inductors and this supported the validation of this model. There is no change in Rs, Ls, Cox and Csub, which is translated to the fact that the resonant frequency will not be changed. A simultaneously impressive increase of 3 ~ 4 orders in magnitude for Rsub and Rc has been evidenced, namely, from 10^2 Ω to 10^5 ~ 10^6 Ω for Rsub and from 10^1 Ω to 10^4 ~ 10^5 Ω for Rc, respectively. This translates to the fact that the substrate loss and coupling can be neglected. This suggests that the bombarded inductor indeed improves the Si substrate loss, resulting in a higher Q-value and better frequency response of the spiral inductors. The slightly change in Rp and Cs may be due to the change in the substrate return path after the bombardment and needs to be clarified.

Table II Extracted equivalent inductor circuit parameter, with and without bombardment.

Parameter	w/i bombardment			w/o bombardment		
N	1.5	2.5	3.5	1.5	2.5	3.5
Rsub1,2 (KΩ)	*1517*	*872.5*	*193.6*	*0.31*	*0.285*	*0.253*
Csub1,2 (fF)	26.1	38	45.5	23.1	34.07	46.78
Cox1 (fF)	36.84	68.12	101.3	35.24	69.61	98.21
Cox2 (fF)	33.92	65.64	85.32	32.46	59.93	82.13
Ls (nH)	1.09	2.01	3.53	1.07	2.01	3.57
Rp (KΩ)	2.259	4.801	7.392	1.82	3.755	4.771
Rc (KΩ)	*286.9*	*69.1*	*10.15*	*0.012*	*0.01*	*0.008*
Cs (fF)	3.255	21.01	28.91	1.01	6.004	10.98
Rs (Ω)	1.191	1.901	2.679	1.201	2.063	2.8

V. CONCLUSION

Proton bombardment has been selectively applied to on-chip inductors. An increase in substrate resistivity from 10 Ω-cm up to 10^5 ~ 10^6 Ω-cm has been achieved. The resistivity lifetime has also been verified using a 150°C 1000-hour test without any degradation in order of magnitude. Spiral inductors with various turns in terms of 8-level with 3 μm-thick top Cu-interconnect and 6-level with 2 μm-thick top Al-interconnect using TSMC 0.13μm and 0.18μm RF CMOS processes have been realized and bombarded with high energy proton. Characterization based on the S-Parameter measurement demonstrated significant improvements both in high peak Q-value and better frequency response. A maximum Q value of more than 20 and 15 is achieved at an optimum frequency as high as 6.5 GHz and 8 GHz in the cases of 0.13μm and 0.18μm. Improvement as high as 50% has been achieved on average for both FOMs. With the model technology, we proved that simultaneously impressive increases in peak Q-value and shifts in the optimal frequency are due to a significantly reduced substrate parasitic effect resulting from higher substrate resistivity. This can be considered as a solution to integrate inductor monolithically on a Si substrate.

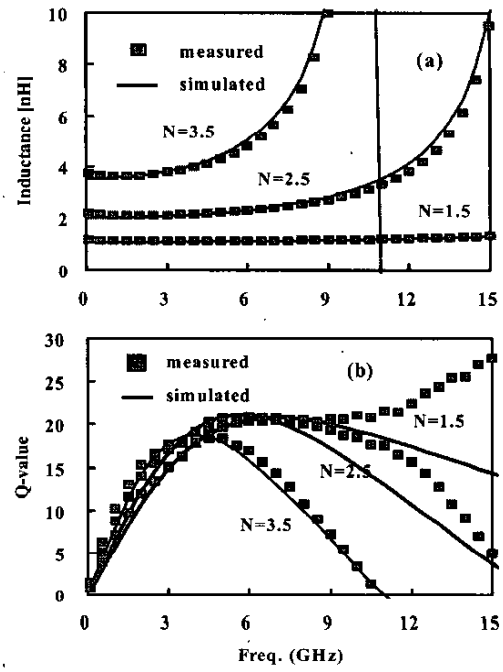

Fig. 4. Measured and simulated inductance (a), and Q-value (b), of inductors with bombardment in the case of 0.13μm.

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